01 / SILICON OVERVIEW

RK3126C

Entry-level display controller · Engineering brief

A legacy 32-bit processor for basic photo, video and touch display designs. Treat it as a cost-oriented baseline; check the software image and lifecycle before choosing it for a new product.

4 × Cortex-A7	Mali-400 MP2	LQFP176

Compute, memory and media

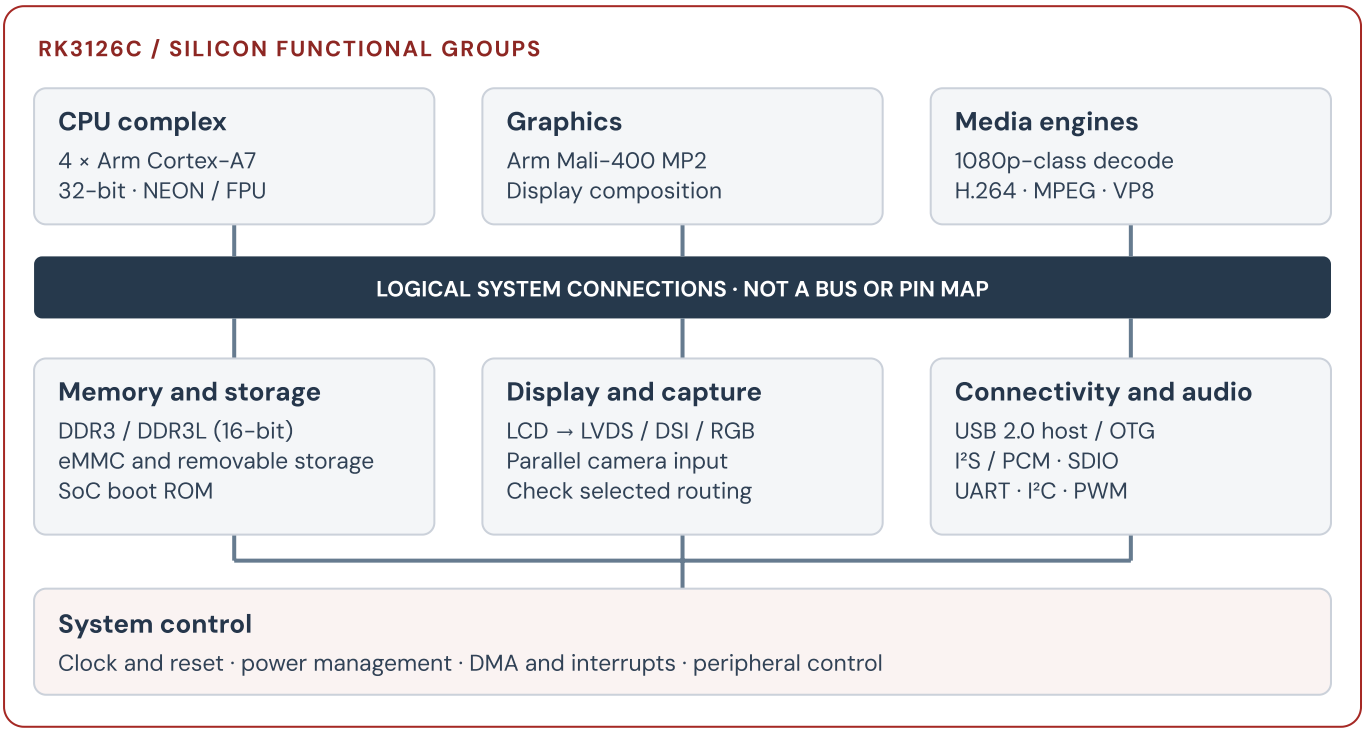
CPU architecture	4 × Arm Cortex-A7 (32-bit)
Graphics	Arm Mali-400 MP2
Package	LQFP176. Confirm body, pitch and pin-1 orientation on the released footprint drawing.
AI accelerator	No dedicated NPU listed in the cited silicon material
Memory interface	DDR3 / DDR3L; 16-bit bus, up to 2 GB address space
Boot and storage	eMMC; removable storage/boot choices depend on board design
Video decode	1080p-class H.264, VC-1, MPEG and VP8; verify profile and frame rate
Video encode	Review codec mode with engineering if capture is required

Framemory product scope: Basic display platform for feasibility review. No released Framemory SKU is asserted.

02 / FUNCTIONAL ARCHITECTURE

SoC Block Diagram

Original diagram grouped by function. Lines indicate logical relationships, not chip topology, package breakout or simultaneous use of interfaces.



Display and interface scope

Panel output	LVDS, MIPI DSI and parallel RGB are silicon-side possibilities
Camera	Parallel camera interface; check supported sensor format and pin allocation
Audio	I²S/PCM and codec-related interfaces; verify board audio routing
USB	USB 2.0 host and USB 2.0 OTG; define host/device roles
Expansion	SDIO or other populated interfaces require exact carrier verification

03 / BOARD DESIGN REVIEW

Board integration

Plan the schematic review around the exact part, PCBA and BSP. These checks are not electrical wiring instructions or production guarantees.

Input power Protection and budget → **Regulators** Rail levels and sequence → **RK3126C** Clock and reset → **Bring-up** DDR, boot and panel

Power domains	Verify core, DDR, I/O and analog rails. Check regulator current headroom, decoupling and shutdown across operating modes.
Reference clock / reset	Check the 24 MHz oscillator reference, reset behavior and regulator sequencing against the exact design.
DDR and storage	Confirm the selected DDR3/DDR3L device, memory initialization and exact eMMC boot and USB recovery paths.
Panel and interfaces	Resolve the pin-mux conflicts and voltage domains for the chosen LCD, parallel camera and SDIO. Verify backlight and touch independently.
Bring-up evidence	Record cold start, reset and recovery. Verify actual interface and media operation on the target firmware under representative load.

Schematic availability: Request the revision-matched schematic, pin map, rail timing and PCB guidelines from Framemory Engineering. No production wiring is included.

Reference

RK3126C silicon datasheet, Rev. 1.1. Specifications describe the component unless noted; they do not guarantee a Framemory product configuration.