01 / SILICON OVERVIEW

# RK3326-S

## Rockchip processor · Engineering brief

64-bit multimedia SoC for embedded displays and photo-frame designs. This brief covers the exact **RK3326-S** variant. It separates component capability from Framemory product configuration.

| 4 × Cortex-A35 | Mali-G31-2EE | TFBGA418L |
|---|---|---|

## Compute, memory and media

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|---|---|
| **CPU / graphics** | 4 × Arm Cortex-A35 (64-bit architecture); Arm Mali-G31-2EE and a separate 2D engine. |
| **Package** | TFBGA418L · 14 × 14 mm body · 0.65 mm ball pitch. Footprint and orientation require the approved package drawing. |
| **Memory** | 32-bit controller; DDR3 / DDR3L / DDR4 / LPDDR3 / LPDDR4, one type per design; up to 4 GB address space per Rev. 1.1. |
| **Boot / storage** | eMMC, SD/MMC and flash interfaces; actual boot source and recovery path depend on the PCBA and image. |
| **Video processing** | H.264 and H.265 decode up to 1080p at 60 fps; H.264 encode up to 1080p at 30 fps. JPEG encode/decode are separate functions. |
| **AI acceleration** | No dedicated NPU listed for this variant. Do not infer neural acceleration from the GPU. |

## Framemory 10P · Selected configuration

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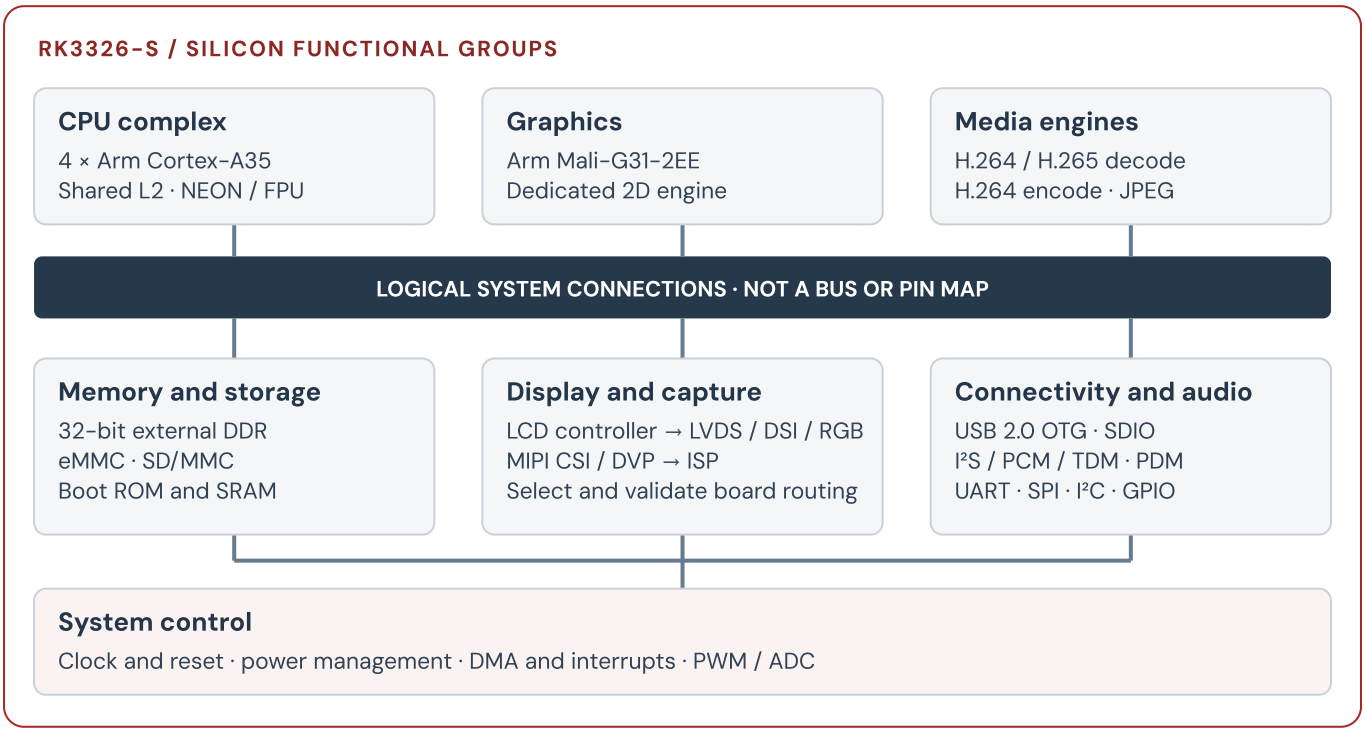
|---|---|
| **Native LCD** | 10.1-inch IPS WXGA · 1280 × 800. |
| **Product playback** | 1080p at 30 fps · H.264 / H.265. This is not the LCD's native resolution. |
| **CPU clock** | 1.5 GHz selected for the 10P specification; verify against the production PCBA and firmware before public release. |

02 / FUNCTIONAL ARCHITECTURE

# SoC Block Diagram

Original engineering diagram grouped by function. Lines indicate logical relationships, not the physical interconnect, package breakout or simultaneous pin use.




## Display and interface limits

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|---|---|
| **LVDS output** | Up to 1280 × 800 at 60 fps per Rev. 1.1; verify mapping and panel timing. |
| **MIPI DSI output** | Up to 1920 × 1080 at 60 fps per Rev. 1.1; verify lane count, bitrate and panel initialization. |
| **Camera input** | CSI or parallel capture and ISP support are silicon-side capabilities. Check exact sensor, pin mux and firmware. |
| **Board interface scope** | USB role, connector count, SDIO module, codec/amplifier and routed panel path depend on the board. |

03 / BOARD DESIGN REVIEW

# Board integration

Use these checkpoints to plan a schematic review. The values, pin assignments and sequencing must come from the approved hardware package for the exact PCBA.

**Input power**
Protection and input budget
→
**PMIC / regulators**
Rail levels and sequence
→
**RK3326-S**
Clock and reset
→
**Board bring-up**
DDR, boot and panel

| | |
|---|---|
| **Power domains** | Map core, DDR, I/O and analog rails to the exact SoC and peripherals. Check sequencing, current headroom, decoupling and shutdown. |
| **Reference clock / reset** | The SoC reference lists a 24 MHz input. Match oscillator network, reset polarity/timing and PMIC power-good to the approved design. |
| **DDR and storage** | Confirm the populated DDR type, layout rules and BSP training parameters. Check eMMC I/O voltage, boot configuration and recovery access. |
| **Panel / touch** | Match the selected interface to panel timings and lane mapping. Check panel power, backlight enable/PWM and the separate touch-control bus. |
| **Bring-up evidence** | Capture cold start, reset and recovery; verify the production image reports the expected CPU operating point. Test video, display and peripherals under load. |

**Schematic availability:** Request the revision-matched reference schematic, power-sequence requirements, ball map and PCB guidelines from Framemory Engineering. No 10P production schematic or verified wiring is included.

## References


- Rockchip RK3326-S Rev. 1.1: silicon and package facts