01 / SILICON OVERVIEW

RK3562

Connected display and lightweight edge AI · Engineering brief

A 64-bit platform for connected displays, camera-enabled products and modest local inference. Evaluate display, camera, AI runtime and performance on the chosen PCBA/BSP together.

4 × Cortex-A53	Mali-G52 2EE	FCCSP478L

Compute, memory and media

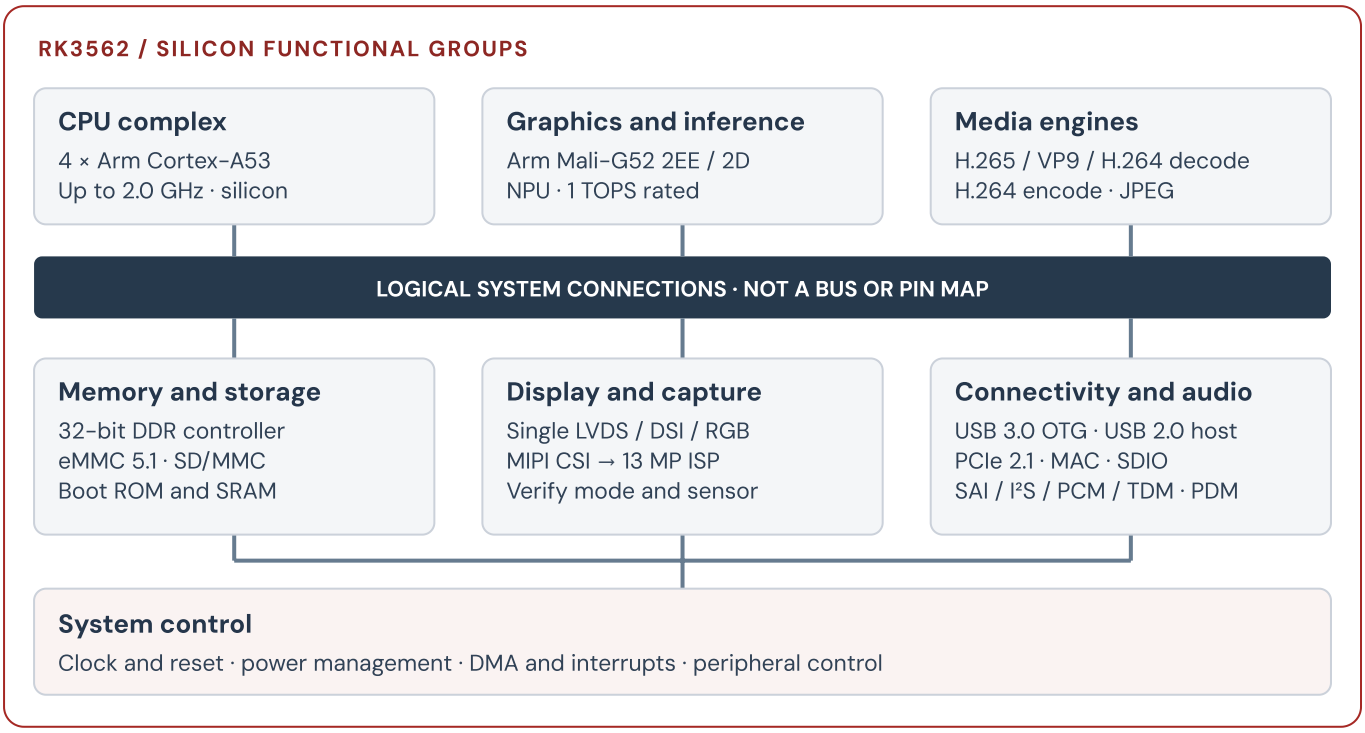
CPU architecture	4 × Arm Cortex-A53, up to 2.0 GHz (Rockchip RK3562)
Graphics	Arm Mali-G52 2EE plus dedicated 2D acceleration
Package	FCCSP478L · 13.9 × 13.9 mm body · 0.50 / 0.65 mm mixed pitch. Use the approved land pattern.
AI accelerator	1 TOPS vendor rating; actual throughput depends on model and runtime
Memory interface	DDR3 / DDR3L / DDR4 / LPDDR3 / LPDDR4 / LPDDR4X
Boot and storage	eMMC supported on module implementations; confirm actual capacity and boot target
Video decode	H.265 / VP9 up to 4K at 30 fps; H.264 up to 1080p at 60 fps
Video encode	H.264 up to 1080p at 60 fps

Framemory product scope: Connected display candidate. No released product configuration, clock setting or BSP is implied.

02 / FUNCTIONAL ARCHITECTURE

SoC Block Diagram

Original diagram grouped by function. Lines indicate logical relationships, not chip topology, package breakout or simultaneous use of interfaces.



Display and interface scope

Panel output	Single display; LVDS, MIPI DSI or parallel RGB
Camera	13 MP ISP rating; sensor, interface and transport must be validated together
Audio	SAI with I²S/PCM/TDM and PDM capability; verify channel use
USB	USB 3.0 OTG and USB 2.0 host
Expansion	PCIe 2.1; RGMII / RMII MAC interfaces, with board PHY/routing as applicable

03 / BOARD DESIGN REVIEW

Board integration

Plan the schematic review around the exact part, PCBA and BSP. These checks are not electrical wiring instructions or production guarantees.

Input power	→	Regulators	→	RK3562	→	Bring-up
Protection and budget		Rail levels and sequence		Clock and reset		DDR, boot and panel

Power domains	Verify core, DDR, I/O and analog rails. Check regulator current headroom, decoupling and shutdown across operating modes.
Reference clock / reset	Check the 24 MHz reference and power-good/reset behavior. Confirm voltage and power-state settings for standard RK3562, not RK3562J.
DDR and storage	Confirm the populated DDR type/width, training and PCB constraints, eMMC mode and fallback recovery.
Panel and interfaces	Validate the selected panel and sensor at the same time. Check PCIe/USB use and any mux limits; confirm the external Ethernet PHY and clocking.
Bring-up evidence	Record cold start, reset and recovery. Verify actual interface and media operation on the target firmware under representative load.

Schematic availability: Request the revision-matched schematic, pin map, rail timing and PCB guidelines from Framemory Engineering. No production wiring is included.

Reference

RK3562 silicon datasheet, Rev. 2.1. Specifications describe the component unless noted; they do not guarantee a Framemory product configuration.