01 / SILICON OVERVIEW

RK3572

Advanced multimedia and edge AI · Engineering brief

An eight-core platform for richer display pipelines and local AI. Use the published SoC capability as a screening reference, then size the board and software against the required concurrent workload.

2 × A73 + 6 × A53	Mali-G310V2	FCCSP550L

Compute, memory and media

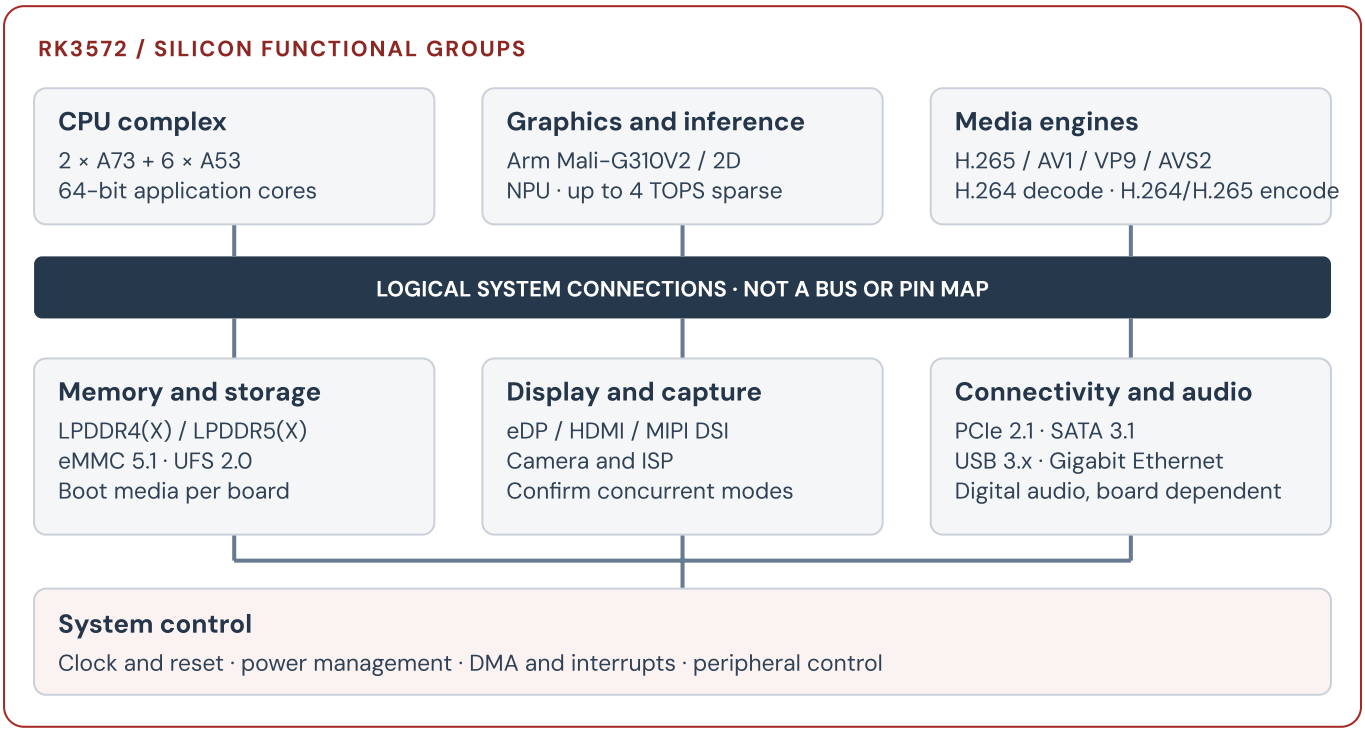
CPU architecture	2 × Arm Cortex-A73 + 6 × Cortex-A53; 64-bit
Process / graphics	8 nm; Arm Mali-G310V2 and dedicated 2D acceleration
Package	FCCSP550L · 14.3 × 15.5 mm body · 0.42 / 0.52 / 0.65 mm mixed pitch. Use the approved land pattern.
AI accelerator	Up to 4 TOPS sparse (vendor rating); model conditions apply
Memory interface	LPDDR4 / LPDDR4X / LPDDR5 / LPDDR5X per silicon reference; verify board choice
Boot and storage	eMMC 5.1 / UFS 2.0 listed; confirm boot support by design
Video decode	Vendor's detailed product table gives a 4K/60 fps ceiling for listed formats; verify per codec
Video encode	Vendor's detailed product table lists H.264 / H.265 up to 4K at 40 fps

Framemory product scope: Advanced platform candidate for evaluation. No released Framemory SKU or ship date is asserted.

02 / FUNCTIONAL ARCHITECTURE

SoC Block Diagram

Original diagram grouped by function. Lines indicate logical relationships, not chip topology, package breakout or simultaneous use of interfaces.



Display and interface scope

Panel output	eDP / HDMI / MIPI DSI; multi-display support is topology dependent
Camera	12 MP ISP rating per launch material; confirm sensor paths
Audio	Validate digital audio routing, external codec and BSP support
USB	USB 3.x advertised; verify available ports and lane-sharing on the selected board
Expansion	PCIe 2.1 / SATA 3.1 and Gigabit Ethernet; check shared lanes and external PHYs

03 / BOARD DESIGN REVIEW

Board integration

Plan the schematic review around the exact part, PCBA and BSP. These checks are not electrical wiring instructions or production guarantees.

Input power Protection and budget → **Regulators** Rail levels and sequence → **RK3572** Clock and reset → **Bring-up** DDR, boot and panel

Power domains	Verify core, DDR, I/O and analog rails. Check regulator current headroom, decoupling and shutdown across operating modes.
Reference clock / reset	Check the 24 MHz reference input, rail sequencing, reset and supported low-power states with the approved board documentation.
DDR and storage	Validate the populated LPDDR generation and training. Confirm whether eMMC or UFS is fitted, supported for boot, and recoverable.
Panel and interfaces	Confirm shared lanes and clocking for the selected PCIe, SATA, USB and display modes. Check concurrent decode, display and AI under sustained thermal load.
Bring-up evidence	Record cold start, reset and recovery. Verify actual interface and media operation on the target firmware under representative load.

Schematic availability: Request the revision-matched schematic, pin map, rail timing and PCB guidelines from Framemory Engineering. No production wiring is included.

Reference

RK3572 silicon datasheet, Rev. 1.1. Specifications describe the component unless noted; they do not guarantee a Framemory product configuration.